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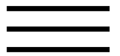

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Test-access mechanism optimization for core-based three-dimensional SOCs â˜† â˜†

Xiaoxia Wu [a] ... Yuan Xie [b]

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Abstract

Embedded cores in a core-based system-on-chip (SOC) are not easily accessible via chip I/O pins. Test-access mechanisms (TAMs) and test wrappers (e.g., the IEEE Standard 1500 wrapper) have been proposed for the testing of embedded cores in a core-based SOC in a modular fashion. We show that such a modular testing approach can also be used for emerging three-dimensional integrated circuits based on through-silicon vias (TSVs). Core-based SOCs based on 3D IC technology are being advocated as a means to continue technology scaling and overcome interconnect-related bottlenecks. We present an optimization technique for minimizing the post-bond test time for 3D core-based SOCs under constraints on the number of TSVs, the TAM bitwidth, and thermal limits. The proposed optimization method is based on a combination of integer linear programming, LP-relaxation, and randomized rounding. It considers the Test Bus and TestRail architectures, and incorporates wire-length constraints in test-access

optimization. Simulation results are presented for the ITC 02 SOC Test Benchmarks and the test times are compared to that obtained when methods developed earlier for two-dimensional ICs are applied to 3D ICs. The test time dependence on various 3D parameters (e.g. 3D placement, the number of layers, thermal constraints, and the number of TSVs) is also studied.

Keywords

Three-dimensional integration; Through silicon via; Test access mechanism; Integer linear programming; Randomized rounding

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